REMARKS

The foregoing amendment amends the title of the application and claims 1, 9, 11 and 16. Pending in the application are claims 1-20, of which claims 1, 9, 11 and 16 are independent. The following comments address all stated grounds for rejection and place the presently pending claims, as identified above, in condition for allowance.

Claim 1 is amended in line 9 to change the phrase "second register file a first thread" to the phrase ---second register file where a first thread---. Claim 1 is also amended to specify that, in a multi-thread mode, a first thread has *exclusive* access to the first register file and a second thread has *exclusive* access to the second register file.

Claim 9 is amended to clarify that a single register name is mapped to both the first and second register files, so that the first and second register files have the same contents.

Claim 11 is amended to specify that respective threads that are simultaneously executing in a multi-thread mode are provided with *exclusive* access to separate respective ones of the register sets.

Claim 16 is amended to clarify that, as a result the first register file and the second register file hold identical contents. *No new matter is added.*

Amendment of the claims is not to be construed as an acquiescence to any of the objections/rejections set forth in the instant Office Action or any previous Office Action, and is done solely to expedite prosecution of the application. Applicants reserve the right to pursue the claims as originally filed, or similar claims, in this or one or more subsequent patent applications.

Objection to Specification:

The title to the invention is objected to as non-descriptive. The foregoing amendment amends the title of the application to: MICROPROCESSOR AND METHOD FOR GIVING EACH THREAD EXCLUSIVE ACCESS TO ONE REGISTER FILE IN A MULTI-THREADING MODE AND FOR GIVING AN ACTIVE THREAD ACCESS TO MULTIPLE

REGISTER FILES IN A SINGLE THREAD MODE, which the Applicants submit is descriptive of the invention. Accordingly, Applicants respectively request the Examiner to reconsider and withdraw the objection to the specification.

Claim Objections

Regarding the objection to claim 1, Applicants have amended claim 1 to include the word "where", as requested by the Examiner, and request that the objection to claim 1 be reconsidered and withdrawn.

35 U.S.C. §102 Rejections

In the Office Action, the Examiner rejects claims 9 and 10 under 35 U.S.C. §102(b) as being anticipated by the previously cited Levy reference (U.S. Patent Number 6,092,175). Applicants traverse the rejection and submit that claims 9 and 10 distinguish patentably over the cited Levy reference. The Levy reference does not teach or suggest register files having registers with identical contents, or the same logical register name, in any mode, as recited in claim 9. The Levy reference also does not teach or suggest a processor capable of transitioning between different modes, in particular between a single thread mode and a multi-thread mode, as also recited in claim 9.

The Levy reference, which is directed to a scheme for sharing of resources between multiple threads executing in a multithreaded processor, does not disclose a processor capable of switching between a multi-thread mode and a single-thread mode, as set forth in the present invention. Rather, the Levy reference only discloses different sharing schemes for a *multi*-threading processor that executes in a multi-thread mode. The processor of Levy is not capable of switching from a multi-thread mode, where each thread has exclusive access to a single register, to a single-threading mode in which a *single* thread is active and the thread has access to all of the available register files, as set forth in the claimed invention. The different embodiments of the multi-thread processor in Levy are mutually exclusive, and a processor is not capable of switching between the different sharing schemes or operating in different modes.

According to the Examiner, because the Levy reference discloses an embodiment where a single thread executes, the Levy reference encompasses a processor that switches between a

multi-thread mode and a single-thread mode. However, the Levy reference clearly does not disclose that the availability of registers to a particular thread depends on the mode in which the processor executes or the number of threads executing. Rather, the processor of Levy has the same operation and function regardless of the number of executing threads. Even when the processor of a particular embodiment in Levy operates with a single thread, the processor and register files have the same operation and configuration as when multiple threads are executing. Thus, Levy does not disclose any change depending on the number of threads executing.

According to the Examiner, the register handler 28 of Levy is a mapping mechanism. However, the register handler only determines the registers that will be used and maps references to the selected registers, and does not map references based on whether a single or multiple threads are executing, as set forth in claim 9.

In particular, the Levy reference does not disclose a mapping mechanism that maps a logical register name to registers in both the first register file and the second register file, so that first and second register file hold *identical* contents when in a single thread mode. Each register in Levy does not share the same logical register name when shared, nor are the contents of the register files identical. In fact, the Levy reference fails to disclose that the contents of the register files changes depending on the number of threads executing on a processor.

The Levy reference merely discloses the ability to increase the number of available renaming registers under certain operating conditions. The microprocessor of Claim 9 has a structure, and an operation and a function different from that of the microprocessor disclosed by the Levy reference. Accordingly, the Levy reference does not anticipate Claims 9 and 10.

35 U.S.C. §103 Rejections

In the Office Action, the Examiner rejects claims 1-3, 6-8, 11-13, 15, 16 and 18-20 under 35 U.S.C. §103(a) as being unpatentable over Levy in view of Cook (U.S. Patent Number 5,301,340). The Examiner also rejects claims 4, 5 and 14 under 35 U.S.C. §103(a) as being unpatentable over the Levy reference in view of the Cook reference and the Sollars reference (U.S. Patent Number 5,900,025). Applicants respectfully traverse the rejection of claims 1-8,

11-16 and 18-20 under 35 U.S.C. §103 and submit that the claims distinguish patentably over the cited references. Even in combination, the cited references fail to disclose the subject matter of claims 1-8, 11-16 and 18-20. Moreover, Applicants submit that motivation to modify and/or combine the teachings of the Levy reference, the Cook reference and/or the Sollars reference is lacking. Therefore, a *prima facie* case of obviousness has not been made, and the rejection should be reconsidered and withdrawn.

The cited references, alone or in combination, fail to disclose a microprocessor capable of switching between different modes, as recited in independent claims 1, 11 and 16. As described above, the Levy reference in particular does not disclose a microprocessor capable of switching between different modes. Rather, the Levy reference discloses different, mutually exclusive embodiments of a multi-threading processor that shares resources. There is no teaching or suggestion that the processor of Levy is capable of switching between different modes, in particular between a single thread mode, where a *single* thread executes and has access to multiple registers and a multi-thread mode, wherein a plurality of threads execute, and each thread has *exclusive* access to a register.

In certain embodiments of Levy, *multiple* threads share one or more register files, as described in column 10, lines 5-61. In an alternate embodiment, the "Private Architectural and Private Renaming (PAPR) scheme, each thread has a dedicated register file, and each thread only access registers from its own context, as described in column 9, line 52-column 10, line 4. There is no teaching or suggestion that the processor can switch between the different embodiments, or that the sharing of register files depends on the number of threads executing on the processor.

However, even if the Levy reference did disclose that the processor was capable of switching between different embodiments, the Levy reference fails to disclose that the availability of a register to an executing thread depends on the number of threads executing on a processor.

In addition, as recognized by the Examiner, the Levy reference also fails to disclose renaming a register name in a single thread mode to refer to a first location in a first register file

and to a first location in a second register file, as recited in independent claims 1, 11 and 16. According to the Examiner, because the Cook references discloses broadcasting data written by an ALU to a plurality of register files, claims 1-3, 6-8, 11-13, 15, 16 and 18-20 are obvious.

However, the Cook reference does not compensate for the deficiencies of the Levy reference. The Cook reference is directed to a computer architecture including parallel arithmetic logic unit (ALUs), each provided with an associated register file. As described in column 4, lines 44-47, the invention of Cook allows for data written by an ALU to be shared with all four register files in the computer architecture. The Cook reference therefore merely discloses that information can be shared amongst different register files, but does not disclose that a single register name is renamed to refer to a location in a plurality of files or that different register files can have the same contents. Therefore, even in combination, the references fail to anticipate the claimed invention.

The Sollars reference, which is directed to a processor including a plurality of control registers organized in a hierarchy, also does not compensate for the deficiencies of the Levy reference and the Cook reference. The Sollars reference also does not disclose a microprocessor that includes a single-thread mode in which a register name is renamed to refer to a first location in a first register file and to a first location in a second register file, nor a microprocessor capable of switching between modes and allocating registers depending on a number of threads executing.

Furthermore, Applicants maintain that even though the combination of the references fails to anticipate the claimed invention, motivation to combine and/or modify the teachings of the different references is lacking. Under U.S. law, even if a combination of the references teaches every element of the claimed invention, without a motivation to combine, a rejection based on a *prima facie* case of obvious is improper. The Examiner states that quick performance would provide motivation to combine and/or modify the teachings of the cited references. However, the Examiner has not provided an objective reason to combine the references found from the references themselves. Therefore, a *prima facie* case of obviousness has not been established, and the rejection should be withdrawn.

In determining whether a case of *prima facie* obviousness exists, it is necessary to ascertain whether the prior art teachings would appear to be sufficient to one of ordinary skill in the art to suggest making the claimed substitution or other modification. The prior art must provide the motivation to make a change to its own teachings to arrive at the invention under rejection. That is, it is not sufficient that the prior ***could be*** so modified; instead the prior art must teach or suggest that the prior art ***should be*** so modified.

Applicants submit that the cited references lack motivation for making the combination, and that the invention is not obvious.

It is well-established law that the motivation to modify the teachings of a reference or to combine references must come from the references themselves, and cannot be derived from the teachings of the application under examination. However, none of the cited references, alone or in combination, teaches or suggests the claimed invention, or provide any motivation for modification or combination of their teachings. As is evident from a close reading of the references and a comparison to the pending claims, the instant rejection constitutes nothing more than a picking and choosing of the various elements of the claims from a number of references based, not on motivation from the references themselves, but rather based on the teachings of the application. Thus, the instant rejection constitutes an impermissible hindsight reconstruction of the invention.

For at least these reasons, the rejection of claims 1-3, 6-8, 11-13, 15, 16 and 18-20 should be reconsidered and withdrawn.

CONCLUSION

In view of the above amendment, applicant believes the pending application is in condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue. If, however, the Examiner considers that obstacles to allowance of these claims persist, we invite a telephone call to Applicant's representative.

Applicant believes no fee is due with this amendment. However, if a fee is due, please charge our Deposit Account No. 12-0080, under Order No. SMQ-021 from which the undersigned is authorized to draw.

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Respectfully submitted,

By _____

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